What is claimed is:

1. A method of analyzing the amount of electromagnetic interference of LSI by executing a logic simulation, the method including the steps of:

allocating a discrete FFT analysis frequency width in each frequency range and performing modeling; and

performing high-speed Fourier transform processing on current change information calculated by the modeling step.

2. An electromagnetic interference analysis method according to claim 1, wherein the modeling step includes:

a discrete analysis frequency width change specifying step for specifying in a particular frequency range a change in a discrete high-speed Fourier transform (FFT) analysis frequency width; and

a modeling process for allocating different discrete FFT analysis frequency widths to the specified frequency range and to a frequency range other than the specified frequency range and performing modeling.

3. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes a step of calculating a current frequency component simultaneously with the calculation at each point in time of a current of a circuit to be analyzed for electromagnetic interference.

4. A method of analyzing the amount of electromagnetic

interference by executing a logic simulation, according to claim 1, wherein the modeling step includes a step of calculating a current frequency component for a time interval each time the current calculation is performed for that time interval, the time interval being less than a time range of an object to be analyzed, and then calculating current frequency components for the entire time range of the object based on the calculated current frequency component.

5. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step has:

a current frequency component storage step; and

a current frequency component calculation step for storing in the current frequency component storage means only those current frequency component values in excess of a predetermined threshold.

6. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step has:

a current frequency component storage step; and

a current frequency component calculation step for storing in the current frequency component storage means only a predetermined number of current frequency component values in the order of magnitude.

7. A method of analyzing the amount of electromagnetic

interference by executing a logic simulation, according to claim 1, wherein the modeling step includes:

a step of calculating a current frequency component for only a predetermined circuit portion in a network to be analyzed.

8. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes:

a step of calculating a current frequency component for only those circuit portions in an object network having one or more circuit portions whose currents are estimated to exceed a predetermined threshold.

9. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes:

a step of calculating a current frequency component for only a predetermined number of circuit portions that are selected in the order of estimated current magnitude from an object network having two or more circuit portions.

10. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes:

a step of calculating a current frequency component for only those circuit portions in an object network having one or more circuit portions whose logic change numbers exceed a

predetermined threshold.

11. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes:

a step of calculating a circuit frequency component for only a predetermined number of circuit portions that are selected in the order of logic change number from an object network having one or more circuit portions.

12. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, wherein the modeling step includes:

a step of estimating from network information the number of logic changes in an object network; and

a step of calculating a current frequency component for those circuit portions that are selected based on the number of logic changes from the object circuit having one or more circuit portions.

13. An apparatus for analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1,the apparatus including:

a means as a user interface for identifying, from a result of performing FFT on a current waveform for each instance, an instance name which mainly causes noise in an associated frequency component with large noise.

14. An apparatus for analyzing the amount of

electromagnetic interference by executing a logic simulation, according to claim 1,the apparatus including:

a means as a user interface for identifying, from a result of performing FFT on current waveforms for each instance group consisting of one or more instances, an instance group which mainly causes noise in an associated frequency component with large noise.

15. An apparatus for analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1,the apparatus including:

a means as a user interface for grouping instances according to flag information written in library or for grouping them into instance groups of registers, combined circuits and memories.

16. An apparatus for analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1,the apparatus having:

a means as a user interface for grouping instances according to whether the instances belong to a clock tree connected to each clock input terminal.

17. An apparatus for analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1, the apparatus including:

a means as a user interface for grouping instances according to a result of identifying the timing at which status

changes occur simultaneously or in a predetermined time duration.

18. An electromagnetic interference analysis apparatus according to claim 15, wherein the grouping means includes:

a means for identifying, from the instance grouping information, an instance name which mainly causes noise in an associated frequency component with large noise and then reporting information on noise level.

19. An apparatus for analyzing the amount of electromagnetic interference by executing a logic simulation, according to claim 1,the apparatus including:

a means as a user interface for performing FFT only on a predetermined frequency.

20. A method of analyzing the amount of electromagnetic interference of LSI by executing a logic simulation, the method including a current waveform correction step, the current waveform correction step comprising:

a step of calculating an equivalent resistance and an equivalent capacitance of an entire chip from a resistance and a capacitance of a power supply circuit of the chip that were determined by performing LPE based on layout data, and calculating a correction coefficient; and

a step of correcting, by using the correction coefficient, an event-based model of an estimated current waveform obtained in advance as an ideal power supply.

21. An electromagnetic interference analysis method according to claim 20, wherein the correction coefficient calculation step includes a step of calculating the equivalent resistance and equivalent capacitance of the entire chip from information on resistance and capacitance of a power supply circuit of the chip and calculating the correction coefficient by performing processing according to a table prepared in advance.

22. An electromagnetic interference analysis method according to claim 20, wherein the correction coefficient calculation step includes a step of calculating the equivalent resistance and equivalent capacitance of the entire chip from information on resistance and capacitance of a power supply circuit of the chip and calculating the correction coefficient by performing processing according to a mathematical expression prepared in advance.

23. An electromagnetic interference analysis method according to claim 20, wherein the correction processing step includes a step of correcting a base of the event-based model of the estimated current waveform obtained as an ideal power supply.

24. An electromagnetic interference analysis method according to claim 20, wherein the correction processing step includes a step of correcting an area of the event-based model of the estimated current waveform obtained as an ideal power

supply.

25. An electromagnetic interference analysis method according to claim 20, wherein the correction coefficient calculation step includes a step of estimating the equivalent resistance of the chip from the resistance information of the power supply circuit by using shape information of the power supply circuit and then performing the correction coefficient calculation step at high speed.

26. A method of analyzing the amount of electromagnetic interference by executing a logic simulation, the method having:

a step of estimating an equivalent resistance and an equivalent capacitance of a power supply circuit of a chip at a floorplan stage;

a step of calculating a correction coefficient from the information on the equivalent resistance and equivalent capacitance; and

a step of correcting an event-based model of an estimated current waveform obtained in advance as an ideal power supply.

27. An electromagnetic interference analysis method according to claim 26, wherein the step of estimating the equivalent resistance and equivalent capacitance includes a step of estimating the resistance and capacitance of the power supply circuit by considering an area of the chip.

28. An electromagnetic interference analysis method

according to claim 27, wherein the step of estimating the equivalent resistance and equivalent capacitance further includes a step of estimating the resistance and capacitance of the power supply circuit by considering technology information.

29. An electromagnetic interference analysis method according to claim 27, wherein the step of estimating the equivalent resistance and equivalent capacitance further includes a step of estimating the resistance and capacitance of the power supply circuit by considering a chip shape and a power supply pad position.

30. An electromagnetic interference analysis method according to claim 27, wherein the step of estimating the equivalent resistance and equivalent capacitance further includes a step of estimating the resistance and capacitance of the power supply circuit by considering the number of power supply pads.

31. An electromagnetic interference analysis method according to claim 27, wherein the step of estimating the equivalent resistance and equivalent capacitance further includes a step of estimating the resistance and capacitance of the power supply circuit by considering information on a width of the power supply wire making up the chip.

32. An electromagnetic interference analysis method according to claim 27, wherein the step of estimating the

equivalent resistance and equivalent capacitance further includes a step of estimating the resistance and capacitance of the power supply circuit by considering a capacitance generation area under the power supply wire.

33. An electromagnetic interference analysis method according to claim 20 , wherein, to consider the power supply wire for each module in a post-layout electromagnetic interference analysis, the current waveform correction step includes a step of calculating an equivalent resistance and an equivalent capacitance for each module, rather than for the entire chip, and calculating a correction coefficient for each module to make corrections to the estimated current waveform more precisely for each module.

34. An electromagnetic interference analysis method according to claim 26, wherein, to consider the power supply wire for each module in a pre-layout electromagnetic interference analysis, the current waveform correction step includes a step of estimating an equivalent resistance and an equivalent capacitance for each module, rather than for the entire chip, by considering information on a position of each module making up the chip and information on a kind of each module and calculating a correction coefficient for each module to make corrections to the estimated current waveform more precisely for each module.

35. An electromagnetic interference analysis method

according to claim 26 , wherein the current waveform correction step includes:

a step of calculating an equivalent resistance and an equivalent capacitance of the entire chip from information on resistance and capacitance of the power supply circuit of the chip and calculating a correction coefficient by using a table or mathematical expression prepared in advance; or

a step of correcting a base or area of an event-based model of the estimated current waveform obtained as an ideal power supply.

36. An electromagnetic interference analysis method according to claim 20 , wherein, to consider an inductance component of a power supply wire in the electromagnetic interference analysis, the current waveform correction step includes:

a step of calculating from package information of the chip an inductance component corresponding to the power supply lead portion and the power supply wire bonding portion and using it as a third element following the resistance and capacitance.

37. An electromagnetic interference analysis method according to claim 20, wherein, to consider an influence of a power supply wire on the current waveform obtained as an ideal power supply in the electromagnetic interference analysis, the current waveform correction step corrects the current waveform obtained as an ideal power supply that is to be analyzed for

electromagnetic interference, instead of correcting an event-based model of the estimated current waveform.